(Knowledge for Development)

KIBABII UNIVERSITY

UNIVERSITY EXAMINATIONS
2022/2023 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR THREE SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF
BACHELOR OF SCIENCE COMPUTER SCIENCE

COURSE CODE : **CSC 353E**

COURSE TITLE : **DIGITAL SYSTEM DESIGN**

DATE: 19 /04/2023 **TIME: 2.00PM-4.00PM**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE (COMPULSORY) **[30 MARKS]**

a) Define "digital system design?' (2 marks)

b) Outline four merits of using Hardware Descriptive Language in digital systems design (4 marks)

c) State three advantages of using PLD over standard chips in design (3 marks)

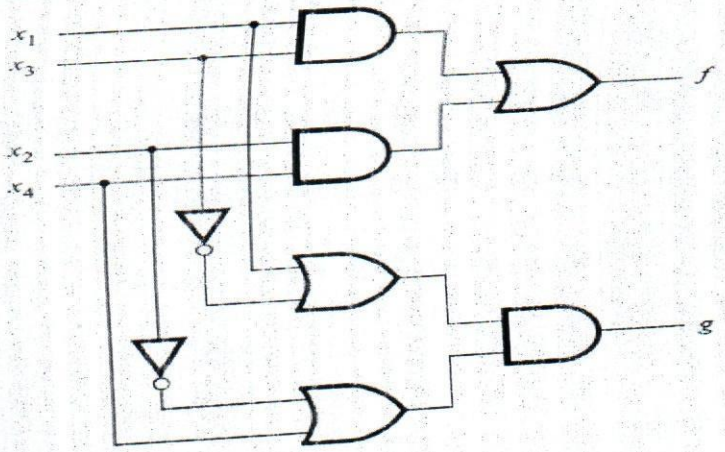
d) Distinguish between the following ways of implementing digital systems: (4 marks)

i) General purpose processors

ii) Special purpose processors

e) Describe the following three phases of physical design: placement, routing and static timing analysis (6 marks)

f) Write the entity and architecture VHDL code of the circuit below: (7 marks)



g) Highlight the following modes of verification of a digital system (4 marks)

i) Simulation

ii) timing analysis

iii) formal verification

iv) hardware emulation

SECTION B

QUESTION TWO

a) Write the entity declaration of the following digital components in VHDL language: (5 marks)

i. Half adder (5 marks)

ii. Full adder

b) Write the architectural declaration of the following digital components in VHDL language: (5 marks)

i. Half adder (5 marks)

ii. Full adder

QUESTION THREE

a) State four advantages of Application Specific ICs chips over PLDs (4 marks)

b) Discuss the following phases of synthesis (6 marks)

i) Netlist generation

ii) Gate optimization

iii) Technology mapping

c) Design a full adder by developing its truth and writing a VHDL code to implement the adder (10 marks)

QUESTION FOUR

a) Discuss the significance of the following tasks in digital system design process: (10 marks)

i) Synthesis
ii) Physical design
iii) Verification
iv) Testing

b) You are required to write a completed VHDL program that assigns signals using WITH _ SELECT_WHEN clauses for a 2-to-1 multiplexer. The multiplexer has w0, w1 and s as input signals and f as output signal. The truth table is shown below (10 marks)

Input, s	Output, f
w0	0
w1	1

QUESTION FIVE

a) Discuss the features of a HDL (6 marks)

b) Distinguish between an entity and an architecture (4 marks)

c) Study the architecture below and describe each line of code: (10 marks)

```
ARCHITECTURE Behavior OF mux2to1 IS
BEGIN
        PROCESS ( w0, w1, s )
        BEGIN
                IF s '0' THEN
                        f <= w0;
                ELSE
                        f <= w1;
                END IF;
        END PROCESS;
END Behavior;
```