(Knowledge for Development)

KIBABII UNIVERSITY

(KIBU)

UNIVERSITY EXAMINATIONS
2022/2023 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR ONE SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF BACHELORS OF SCIENCE
(INFORMATION TECHNOLOGY)

COURSE CODE : BIT 124

COURSE TITLE : DIGITAL ELECTRONICS

DATE: 18/04/2023 **TIME: 9.00 A.M. -11.00 A.M.**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE AND ANY OTHER TWO QUESTIONS

QUESTION ONE (COMPULSORY) [30 MARKS]

i. Differentiate between analog quantities and digital quantities. **[2 marks]**

ii. Solve the Boolean expression F = C(B + C)(A + B + C). **[3 marks]**

iii. a. What is the function of a Karnaugh map? **[2 marks]**

b. State the various kinds of Karnaugh maps. **[3 marks]**

iv. What is a counter? **[2 marks]**

v. Solve the following boolean expression F = ((XY' + XYZ)' + X(Y + XY'))' **[3 marks]**

vi. State the main categories of sequential circuits. **[3 marks]**

vii. State two common features in both latch and flip flop. **[2 marks]**

viii. Differentiate between Synchronous and asynchronous sequential logic circuits. **[2 marks]**

ix. a. What do you understand by the term universal gates? **[2 marks]**

b. Name the different universal gates **[2 marks]**

x. Generate a section of the truth table with respect to seven segment display which is used to display the element for Number '0' hence draw the element 0 **[4 marks]**

QUESTION TWO [20 MARKS]

i. State De Morgan's theorems hence prove them using truth tables. **[6 marks]**

ii. Simplify AB + BC + AC to its Standard Sum of products hence find its min-terms **[3 marks]**

iii. Minimize the logic function $Y(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$ using Karnaugh map method. **[5 marks]**

iv. Draw a truth table and a logic diagram that implements the following expression.

$W=\overline{X+Y}+X\bar{Z}$

[6 marks]

QUESTION THREE [20 MARKS]

i. Differentiate between a serial shift and a parallel shift with respect to registers.

[2 marks]

ii. Define the term shift register. **[2 marks]**

iii. Discuss the finite machine theory. **[3 marks]**

iv. Contrast between combinational logic circuits and sequential logic circuits clearly stating all the differences with respect to their output, memory and fundamental building block **[6 marks]**

v. Generate an OR function using NAND gates only **[3 marks]**

vi. Outline the basic types of registers. **[4 marks]**

QUESTION FOUR [20 MARKS]

i. List the different categories of counters and briefly explain how they work. **[9 marks]**

ii. Generate a JK flip flop using a D flip flop **[11 marks]**

QUESTION FIVE [20 MARKS]

i. Realize an OR function using NOR gates. **[3 marks]**

ii. Explain how the emitter coupled logic functions. **[3 marks]**

iii. State four characteristics that are considered for the selection of a particular logic family.

[4 marks]

iv. Design a two-bit multiplier out of logic gates (i.e. it multiplies two two-bit numbers resulting in a 4-bit number). **[10 marks]**