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UNIVERSITY EXAMINATIONS
2021/2022 ACADEMIC YEAR

SPECIAL/SUPPLEMENTARY EXAMINATIONS
YEAR FOUR SEMESTER ONE EXAMINATIONS

FOR THE DEGREE OF
(COMPUTER SCIENCE)

COURSE CODE : CSC 450E

COURSE TITLE : MICROPROCESSOR SYSTEMS DESIGN

DATE: 16/11/22 **TIME: 11.00 A.M – 01.00 P.M**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE [COMPULSORY - 30 MARKS]

(a) Define the following key terms applicable in microprocessor systems design

(i) Microprocessor **[1 mark]**

(ii) Bus error **[1 mark]**

(iii) System reset **[1 mark]**

(b) State two techniques that eliminate the need for hardware-based interlocking in a pipelined processor **[4 marks]**

(c) A systems engineer wishes to run to a program that is p% perfectly parallelizable on a multiprocessor. Assume there are unlimited number of processing elements. If the maximum speedup achievable on this program is 100, what is p? **[4 marks]**

(d) Super pipelining and superscalar architecture improves performance of the processor. Explain how the two architecture concepts achieve performance improvement. **[4 marks]**

(e) The fundamental distinction between interrupts and exceptions is that interrupts are caused by external events and exceptions are caused by events internal to the running process

(i) Interrupts are handled mostly when convenient. Why? **[2 marks]**

(ii) Why are interrupts not always handled when convenient? Give an example. **[3 marks]**

(f) Suppose you are designing a computer from scratch and that your firms budget allows a very small amount of bandwidth. Which of the following characteristics would you choose in the ISA and the microarchitecture, and why? Explain briefly.

i. Variable length instructions or fixed length instructions? **[2 marks]**

ii. Complex Instructions or simple instructions **[2 marks]**

iii. A large L2 cache or small L2 cache? (L2 is the last level cache) **[2 marks]**

iv. An aggressive prefetcher or a conservative prefetcher? **[2 marks]**

v. Larger cache blocks or small cache blocks? **[2 marks]**

QUESTION TWO [20 MARKS]

(a) Explain how the following techniques are used in improving execution rate of instructions in microprocessor systems

(i) Branch prediction **[2 marks]**

(ii) Speculative execution **[2 marks]**

(b) State five differences between RISC and CISC architecture in microprocessor system design **[5 marks]**

(c) Real-time system performance is determined primarily by the **system response time** and its **data transfer rate.** State the meaning of each of the two-performance metrics in microprocessor system design. **[4 marks]**

(d) Explain the roles of the following two essential units in computer processors

i. Program Flow Control Unit (CU) **[2 marks]**
ii. Execution Unit (EU) **[2 marks]**

(e) State two advantages of RISC over CISC processor systems architecture **[3 marks]**

QUESTION THREE [20 MARKS]

(a) (i) Define the term **embedded system** applicable in microprocessor system design? **[1 mark]**

(ii)List the three components of an embedded system **[3 marks]**

(b) Distinguish between vector and scalar pipeline applicable in processor systems design **[4 marks]**

(c) Using a block diagram, briefly describe the building blocks of a microprocessor in computer systems **[5 marks]**

(d) State and briefly describe three performance considerations for processor system memory **[3 mark]**

(e) Burst Access Mode is a method of achieving performance enhancement in the design of processor system memory. Illustrate how this is practically achieved. **[4 mark]**

QUESTION FOUR [20 MARKS]

(a) Co-processors execute instructions fetched by the primary processor reducing the load on the primary processor. Briefly describe the role of the following types of co-processors;

(i) Floating point co-processor **[2 marks]**

(ii) Graphic Processing Unit **[2 marks]**

b) Explain the following terms in memory hierarchy in contemporary processor systems

(i) Cache Memory **[2 marks]**

(ii) Virtual Memory **[2 marks]**

c) **Frequency scaling** and **voltage scaling** are some of the design techniques that can help in achieving lower power consumption in microprocessor systems. Explain how each of these techniques achieves this goal. **[3 marks]**

d) The two performance factors in cached memory are cache hit and cache miss. Briefly explain the meaning and role of each of the factors **[4 marks]**

e) (i) State three characteristics of RISC processor architecture **[3 marks]**

(ii) List two disadvantages of CISC processor **[2 marks]**

QUESTION FIVE [20 MARKS]

(a) The two types of hazards that hinder occurrence of ideal pipelining are structural and control hazards. Briefly explain how each of these hazards occur. **[3 marks]**

(b) (i) Explain the meaning of cached memory applicable in memory subsystem **[2 marks]**

(ii) State the objective of having cached memory in the memory subsystem **[2 marks]**

(c) Discuss any four factors to be considered and analyzed at the architectural stage during processor selection for a fire alarm **[8 marks]**

(d) Using a simple block diagrams, briefly describe the main building blocks of a microcontroller and its role in computer systems **[5 marks]**

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