(*Knowledge for Development*)

KIBABII UNIVERSITY

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UNIVERSITY EXAMINATIONS

2021/2022 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS

YEAR TWO SEMSTER ONE

FOR THE BACHELORS DEGREE OF

(COMPUTER SCIENCE)

COURSE CODE: CSC 211.

COURSE TITLE: DIGITAL ELECTRONICS II

DATE: 31/01/2022 **TIME:** 09.00 A.M - 11.00 A.M

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE AND ANY OTHER TWO (2) QUESTIONS

QUESTION ONE (COMPULSORY) [30 MARKS]

a) Draw two truth tables illustrating the outputs of a half-adder, one table for the output and the other for the carry. **[4 marks]**

b) Outline **THREE** ways that RAMs are different from ROM **[3 marks]**

c) A 5-bit D/A converter produces $V_{OUT} = 0.2$ V for a digital input of 0001. Find the value of V_{out} for an input of 11111. **[4 marks]**

d) List **TWO** advantages of synchronous sequential logic circuit and **TWO** disadvantages of asynchronous sequential logic circuit? **[2 marks]**

e) Draw the truth table for a 2-to-4 decoder (i.e., 2 control inputs, C_1, C_0, and 4 outputs, P_3, P_2, P_1, P_0) and show how it can be implemented using 2-input NOR and NOT gates. **[4 marks]**

f) What is the difference between latch and flip flop? **[3 marks]**

g) Draw a diagram to illustrate the 2-to-4 decoder can be used to implement a 4-to-1 multiplexer (i.e., 4 inputs, 2 control inputs and 1 output) using only NAND gates for the additional combinational logic required. **[4 marks]**

h) Draw the truth table for an encoder that accepts a sign bit, S, and two magnitude bits X_0, X_1 and gives a three-bit output Y_2, Y_1, Y_0 that are the two's complement encoding of the input. **[3 marks]**

i) Complete the following truth table that describes a single-bit full adder:

C_{IN}	A	B	C_{OUT}	sum
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	1	

where C_{IN} is carry-in, A and B are the input data, C_{OUT} is carry-out and sum is the sum output. Remember to write your answer on the script paper, i.e., not on the question paper. **[3 marks]**

QUESTION TWO [20 MARKS]

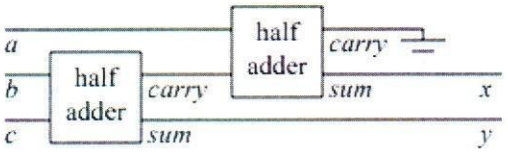
a) Assume the following values for the ADC clock frequency = 1 MHz; V_T =0.1mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values.

i. The digital equivalent obtained for V_A = 3.728 V. **[5 marks]**

ii. The conversion time. **[3 marks]**

iii. The resolution of this converter. **[2 marks]**

b) Fill in the truth table at right for the following circuit. Ignore rows not included in the table. [4mks]



a	*b*	*c*	*x*	*y*
0	1	1		
1	0	1		
1	1	0		
1	1	1		

c) Using only four-bit adders, construct an eight-bit adder. Each four-bit adder has two four-bit inputs and one five-bit output. Your eight-bit adder should have two eight-bit inputs and a one eight-bit output (don't worry about the ninth output bit) **[6 marks]**

QUESTION THREE (20 MARKS)

a) Using two 2-input NOR gates illustrate how to implement an RS latch. Describe it's operation and give its truth table. **[3 marks]**

b) With the aid of a diagram explain what a sequential circuit is. **[4 marks]**

c) Outline **TWO** main differences between synchronous and asynchronous sequential logic circuit? **[4 marks]**

d) With the aid of a diagram, show how a Transparent D-Latch can be implemented using cross-coupled NOR gates and some additional combinational logic. What are the advantages of the Transparent D-Latch over the RS latch? **[5 marks]**

e) The truth table of a 2-to-4-line decoder is presented in the table below.

inputs			outputs			
A1	A0	EN	S3	S2	S1	S0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

What are the minimum sum-of-products equations for each output of the 2-to-4 line decoder? **[4 marks]**

QUESTION FOUR [(20 MARKS]

a) Outline **TWO** advantages and **TWO** disadvantages of R-2R ladder DAC. **[4 marks]**

b) What is the largest value of output voltage from an 8-bit DAC that produces 1.0V for a digital input of 00110010? **[2 marks]**

c) A 2-bit binary adder sums two numbers, A_1A_0 and B_1B_0 to yield the unsigned result $Y_2Y_1Y_0$, where the zero subscript indicates the least significant bit (LSB).

(i) Write down the truth table for the required outputs Y_2, Y_1 and Y_0. **[3 marks]**

(ii) Using a Karnaugh map (K-map) or otherwise, give the simplified sum of products expression for Y_2. **[3 marks]**

(iii) Using a K map or otherwise, determine a simplified product of sums expression for Y_2 and show how the circuit can be implemented using only NOR gates (of any number of inputs). **[4 marks]**

d) A 5-bit DAC has a current output. For a digital input of 101000, an output current of 10mA is produced. What will I_{OUT} be for a digital input of 11101? **[4marks]**

QUESTION FIVE (20 MARKS)

a) Explain the function of a counter in sequential circuits. **[4 marks]**

b) Derive a circuit that implements an 8-to-3 binary encoder **[6 marks]**

c) Outline **TWO** types of each of ADC and DAC. **[4 marks]**

d) State and briefly explain **THREE** performance parameters of D/A converters **[6 marks]**