(Knowledge for Development)

KIBABII UNIVERSITY

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2021/2022 ACADEMIC YEAR

UNIVERSITY EXAMINATIONS

EXAMINATIONS

SPECIAL/SUPPLEMENTARY

EXAMINATIONS

YEAR TWO SEMESTER ONE

EXAMINATIONS

FOR THE BACHELORS DEGREE

COMPUTER SCIENCE

COURSE CODE: CSC 211

COURSE TITLE: **DIGITAL ELECTRONICS II**

DATE: 20/07/2022 **TIME: 11.00 A.M – 01.00 P.M**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE AND ANY OTHER TWO (2) QUESTIONS

QUESTION ONE (COMPULSORY) **[30 MARKS]**

a) Explain **THREE** ways that RAMs are different from ROM [3mks]

b) Outline **TWO** main differences between synchronous and asynchronous sequential logic circuit? [4marks]

c) List **TWO** advantages of synchronous sequential logic circuit and **TWO** disadvantages of asynchronous sequential logic circuit? [4marks]

d) Give the truth table for a 2-to-4 decoder (i.e., 2 control inputs, S1, S0, and 4 outputs, Q_3, Q_2, Q_1, Q_0) and show how it can be implemented using 2-input NOR and NOT gates. [4 marks]

e) There are **SIX** descriptions in the table below. Complete the table by writing the correct storage device or media in the box next to each description [6marks]

Description	Storage device or media
Non-volatile memory that can only be read from and not written to	
Optical storage media that allows very high storage capacity by using blueviolet technology	
Volatile memory that stores data, programs and the parts of the operating system that are currently in use	
Optical device that uses a single spiral track and uses dual layer technology allowing high data storage capacity	
Device that stores data by controlling the movement of electrons within a microchip, there are no moving parts	
Optical storage media that uses concentric tracks allowing writing and reading to take place at the same time	

f) Show how the 2-to-4 decoder in part (c) can be used to implement a 4-to-1 multiplexor (i.e., 4 inputs, 2 control inputs and 1 output) using only NAND gates for the additional combinational logic required. [4 marks]

g) Give the truth table for an encoder that accepts a sign bit, S, and two magnitude bits X_0, X_1 and gives a three-bit output Y_2, Y_1, Y_0 that are the two's complement encoding of the input. [4 marks]

g) Complete the following truth table that describes a single-bit full adder:

C_{IN}	A	B	C_{OUT}	sum
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	
1	0	1	1	
1	1	0	1	
1	1	1	1	

where C_{IN} is carry-in, A and B are the input data, C_{OUT} is carry-out and sum is the sum output. Remember to write your answer on the script paper, i.e. not on the question paper. [2 marks]

h) Show how C_{OUT} in part (f) can be implemented using only NAND gates. [3 marks]

QUESTION TWO [20 MARKS]

a) With the aid of relevant diagrams, show the effect on the output of a combinational logic circuit of a:

(i) static hazard;

(ii) dynamic hazard. [6marks]

a) Show how two 2-input NOR gates can be connected together to implement an RS latch. Describe its operation and give its truth table. [6 marks]

b) Show how a transparent D latch can be constructed using an RS latch and some combinational logic gates. Briefly describe the operation of such a transparent D latch. [4 marks]

c) i) What is clock as used in timing circuits? [1mks]

ii) Describe **TWO** different types of clock? [2mks]

iii) What is the purpose of clock signal? [1mks]

QUESTION THREE [20 MARKS]

a) With the aid of a diagram, show how a Transparent D-Latch can be implemented using cross-coupled NOR gates and some additional combinational logic. What are the advantages of the Transparent D-Latch over the RS latch? [6 marks]

b) The functionality of a 2-to-4 line decoder is presented in the table below.

inputs			outputs			
A1	A0	EN	S3	S2	S1	S0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

c) What are the minimum sum-of-products equations for each output of the 2-to-4 line decoder? [4 marks]

d) How can five 2-to-4 line decoders be used to produce a 4-to-16 line decoder? Illustrate your answer using a circuit diagram. [6 marks]

e) List the drawbacks of binary weighted resistor technique of D/A conversion. [4marks]

QUESTION FOUR [20 MARKS]

a) Outline **TWO** advantages and **TWO** disadvantages of R-2R ladder DAC.[4marks]

b) Draw a combinational circuit of an eight input multiplexer where the inputs

(D_7, D_6, D_5, D_4, D_3, D_2, D_1, D_0)

are each one bit variable. Label the values of inputs and outputs of each gate of the circuit, assuming the eight inputs have the values (1, 0, 0, 1, 1, 1, 0, 0) respectively, and assuming D_1 is selected. [6marks]

c) A 2-bit binary adder sums two numbers, A_1A_0 and B_1B_0 to yield the unsigned result $Y_2Y_1Y_0$, where the zero subscript indicates the least significant bit (LSB).

(i) Write down the truth table for the required outputs Y_2, Y_1 and Y_0.[3marks]

(ii) Using a Karnaugh map (K-map) or otherwise, give the simplified sum of products expression for Y_2. [3marks]

(iii) Using a K map or otherwise, determine a simplified product of sums expression for Y_2 and show how the circuit can be implemented using only NOR gates (of any number of inputs). [4marks]

QUESTION FIVE [20 MARKS]

a) Derive a circuit that implements an 8-to-3 binary encoder [6marks]

b) Explain the operation of basic sample and hold circuit. [4marks]

c) Outline **TWO** types of each of ADC and DAC. [4marks]

d) Define following performance parameters of D/A converters: [6marks]