(Knowledge for development)

KIBABII UNIVERSITY
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UNIVERSITY EXAMINATIONS
2021/2022 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR FOUR SEMESTER ONE EXAMINATIONS

FOR THE DEGREE OF
(COMPUTER SCIENCE)

COURSE CODE : CSC 450E

COURSE TITLE : MICROPROCESSOR SYSTEMS DESIGN

DATE: 19/05/2022 **TIME:** 02.00 P.M – 04.00 P.M

INSTRUCTIONS TO CANDIDATES

ANSWER **QUESTIONS ONE AND ANY OTHER TWO.**

QUESTION ONE (COMPULSORY) [30 MARKS]

(a) Define the following terms applicable in microprocessor systems design?

i. Multi-tasking **[2 marks]**

ii. Context switching **[2 marks]**

iii. Interrupt latency **[2 marks]**

iv. Embedded system **[2 marks]**

(b) (i) State the purpose of the reference bit in a page table entry **[2 marks]**

(ii) The similar function is performed by which bits in a cache's tag store entry? **[2 marks]**

(c) Pipelining increases processor performance if the pipeline is kept full with useful instructions. State two reasons that often prevent the pipeline from staying full with useful instructions **[4 marks]**

(d) In designing a small, 16KB, 2-way set-associative L1 and a large, 32MB, 32-way set associative L3 cache for the next processor, which one of the following design decisions would you make and why? Justify your choice.

(i) Access L1 tag store and data store: in **parallel** or **series** (select one and explain) **[3 marks]**

(ii) Access L3 tag store and data store in **parallel** or **series** (select one and explain) **[3 marks]**

(e) State two types of hazards that hinder occurrence of ideal pipelining and briefly describe their occurrence **[4 marks]**

(f) The challenge to connecting a large number of peripheral devices to the host bus arise from various devices variations. List three device variations and state the solution to this challenge **[4 marks]**

QUESTION TWO [20 MARKS]

(a) Explain how the following techniques are used in improving execution rate of instructions in microprocessor systems

(i) Branch prediction **[2 marks]**

(ii) Speculative execution **[2 marks]**

(b)State five differences between RISC and CISC architecture in microprocessor system design **[5 marks]**

(c) Real-time system performance is determined primarily by the **system response time** and its **data transfer rate.** State the meaning of each of the two-performance metrics in microprocessor system design. **[4 marks]**

(d) Explain the roles of the following two essential units in computer processors

i. Program Flow Control Unit (CU) **[2 marks]**

ii. Execution Unit (EU) **[2 marks]**

(e) State two advantages of **RISC** over **CISC** processor systems architecture **[3 marks]**

QUESTION THREE [20 MARKS]

(a) (i) State the two components that constitutes the cache **[2 marks]**

(ii) Differentiate between split cache and unified cache **[4 marks]**

(b) A cache has block size equal to the word length. What properties of program behavior, which contributes to higher performance if we use the cache, does not help if we use THIS cache? **[3 marks]**

(c) The performance of real-time systems is determined primarily by the system response time and its data transfer rate. Briefly describe each of the two-performance metrics. **[4 marks]**

(d) The architecture of the input/output device consists of several components. Briefly illustrate diagrammatically the structure and describe the various key components **[7 marks]**

QUESTION FOUR [20 MARKS]

(b) Explain how the following two design techniques can help in achieving lower power consumption in microprocessor systems.

i. Voltage scaling **[2 marks]**

ii. Frequency scaling **[2 marks]**

(c) (i) List three performance metrics for microprocessor system memory **[3 marks]**

(ii) Explain the nature of data that is stored in cached memory in the memory subsystem **[2 marks]**

(iii) State the objective of having cached memory in the memory subsystem **[2 marks]**

(d) State two types of co-processors and briefly describe the role of each in execution of instructions fetched by the primary processor to reduce the load on the primary processor **[5 marks]**

(e) The two performance factors in cached memory are **cache hit** and **cache miss**. Briefly explain the meaning and role of each of the factors **[4 marks]**

QUESTION FIVE [20 MARKS]

(a) Distinguish between the following pipelining techniques in processor systems design

(i) Scalar pipelining **[2 marks]**

(ii) Vector pipelining **[2 marks]**

(b) Memory interleaving increases memory bandwidth by allowing simultaneous access to more than one chunk of memory. State the limitation of this performance enhancement design concept **[2 marks]**

(c) Placement policy is one of the cache management policies where in the cache a block copied in from memory may be placed. Briefly explain how this is implemented in the following three ways;

i. Direct mapping **[2 mark]**
ii. Fully associative **[2 mark]**
iii. Set associative **[2 mark]**

(d) Briefly describe the following standard communication interfaces in processor systems

i. Ethernet LAN Interface **[2 mark]**
ii. Universal Serial Bus (USB) **[2 mark]**
iii. 802.11 Wireless LAN **[2 mark]**
iv. Infrared interface standard (IrDA) **[2 mark]**