(*Knowledge for Development*)

KIBABII UNIVERSITY

UNIVERSITY EXAMINATIONS
2016/2017 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR THREE SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF
COMPUTER SCIENCE

COURSE CODE : CSC 353E

COURSE TITLE : DIGITAL SYSTEM DESIGN

DATE: 28/09/2017 TIME: 11:30 A.M – 1:30 P.M

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO

1) a) State three limitations of a digital system over an analogue system. (3 marks)

b) State two significances of timing analysis as system verification approach. (2 marks)

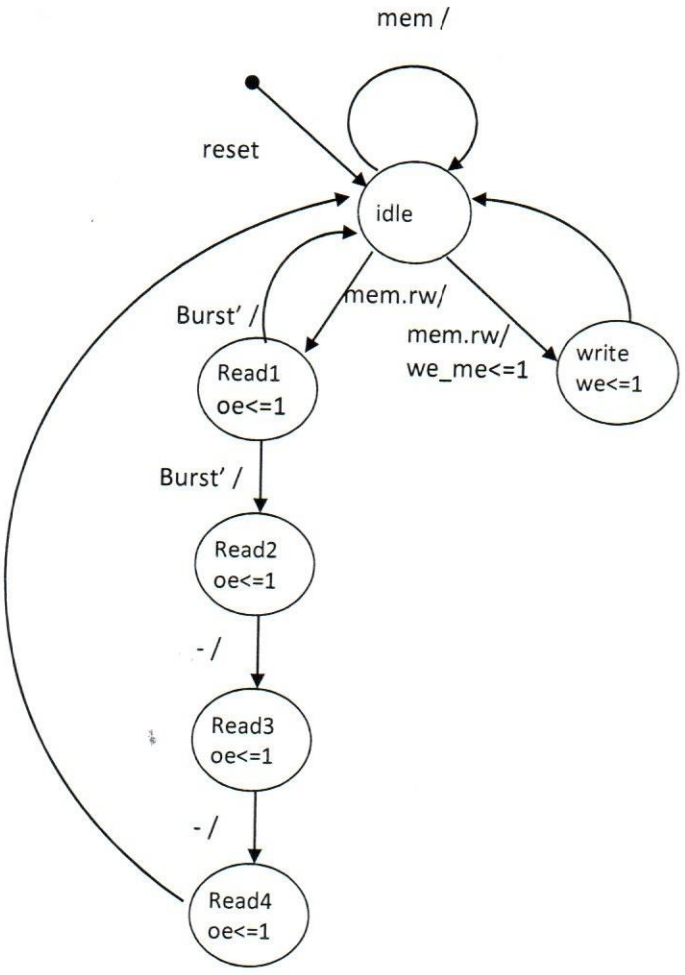
c) Discuss the benefits of using general purpose hardware such as general purpose processors in implementing digital systems. (3 marks)

d) State how HDL differs from other software programming languages (2 marks)

e) Below is the table of a 4-to-1 multiplexer. Using IF-statements, write the process architecture in HDL of the multiplexer. (6 marks)

Inputs	Output x
00	a
01	b
10	c
11	d

f) The figure below shows a FSM diagram. Draw the equivalent ASM chart.(5marks)



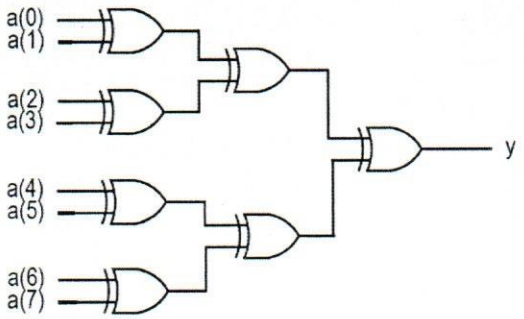
g) Describe the characteristic parameters outlined below for Gate implementation technologies: (5 marks)

i) Fan-in
ii) Noise margin
iii) Propagation delay
iv) Cost of a gate

h) Distinguish between behavioural view and physical view of a digital design stage. (4 marks)

2) a) Draw a block diagram of the transmitter of a wireless digital communication system. Discuss the main stages which the signal undergoes from analogue input to digital transmission. (10 marks)

b) Below is a combinational circuit design implementing reduced_xor circuit. Using ieee standard logic version 1164, write a HDL to realize the implementation. (10 marks)



3) a) Explain the characteristics, listed below, of digital circuit: (8 marks)

i) Entity
ii) Connectivity
iii) Concurrency
iv) Timing

b) Highlight the following viable technologies as used in digital system design.

i) Standard cell Application Specific ICs (9 marks)
ii) Gate Array Application Specific ICs
iii) Field Programmable Gate Arrays

c) Discuss the merits and demerits of using Complex Field Programmable Logic Devices in design. (3 marks)

4) a) Discuss the four techniques listed below of verifying a digital system design

i) Simulation (12 marks)
ii) timing analysis
iii) formal verification
iv) hardware emulation

b) Describe the types of synthesis outlined below: (8 marks)

i) High level synthesis
ii) RT level synthesis
iii) Gate level synthesis
iv) Technology mapping

5) a) Below is a table of binary to gray code conversion. Using the *with - select statements,* write a complete HDL for the conversion. (10 marks)

binary code $b_3b_2b_1b_0$	**gray code** $g_3g_2g_1g_0$
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100

b) Outline the design benefits of hierarchical design (10 marks)