(Knowledge for Development)

KIBABII UNIVERSITY

(KIBU)

MAIN CAMPUS

UNIVERSITY EXAMINATIONS

END OF SEMESTER EXAMINATION

2021/2022 **ACADEMIC YEAR**

FIRST YEAR SECOND SEMESTER **EXAMINATION**

FOR THE DEGREE OF BACHELORS OF SCIENCE IN

(INFORMATION TECHNOLOGY)

COURSE CODE: BIT 124

COURSE TITLE: DIGITAL ELECTRONICS

DATE: 11/05/2022 **TIME:** 9.00 A.M. – 11.00 A.M. **2HRS**

INSTRUCTIONS TO CANDIDATES:

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE [COMPULSORY] (30 MARKS)

a) Determine the octal equivalent of 11101.00110101_2 [2 marks]

b) Define the following terms

i) Bit [1 mark]

ii) Byte [1 mark]

c) Solve the following

i) Determine the binary and hex equivalent of $(24.6)_8$ [3 marks]

ii) Determine the binary and octal equivalent of $(B2F.E4)_{16}$ [3 marks]

d) Prove that A + A' = 1 [2 mark]

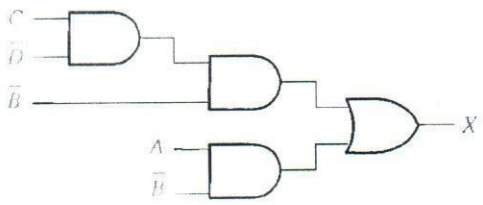
e) Simplify the following Boolean expression below [3 marks]

$$Z = [A\bar{B}(C + BD) + \bar{A}B]C$$

f) Design the logic circuit for the result obtained in 1(e) above [2 marks]

g) Obtain a truth table for the minimized logic circuit in 1(f) above [2 marks]

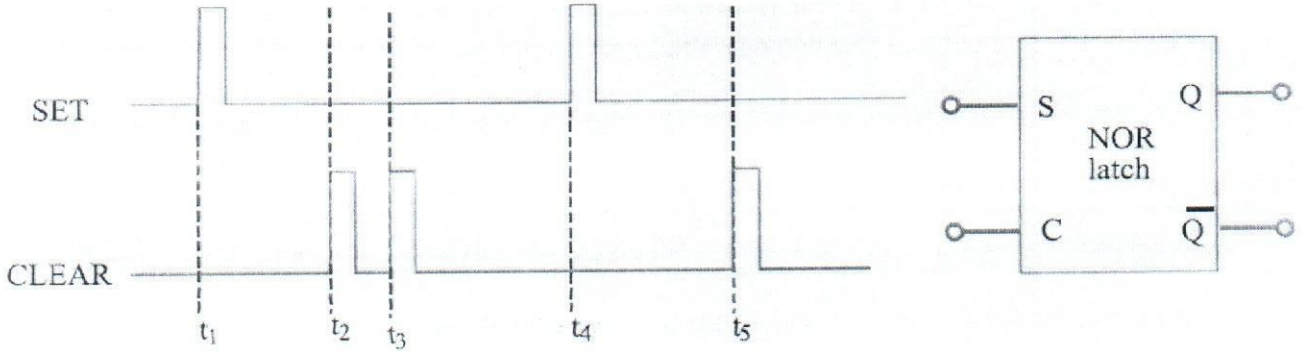
h) Obtain the Boolean expression for the logic circuit given below [3 marks]



i) Simplify the following SOP expression using the Karnaugh mapping technique [5 marks]

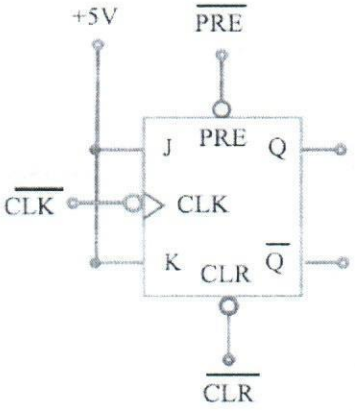
Z = AB + ABC + BC'

j) The waveforms shown in figure below are applied to the inputs of the NOR latch shown, Assume that initially, Q = 0 and determine the Q-waveform. [3 marks]

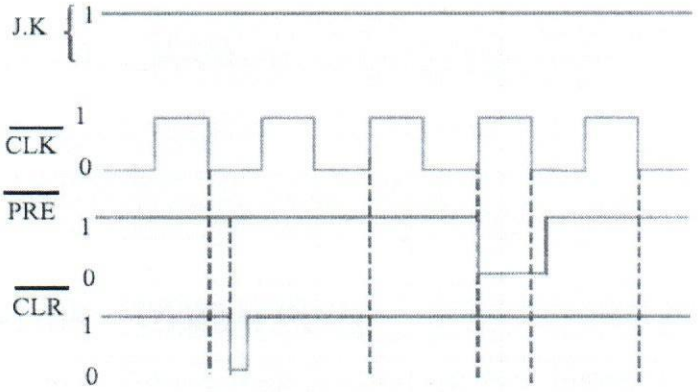


QUESTION TWO [20 MARKS]

a) The Figure (a) below shows the logic symbol for a J-K flip-flop that responds to the falling edge on its clock pulse and has active-LOW asynchronous inputs. The J and K inputs are tied HIGH. Determine the Q-output in response to the waveforms shown in figure (b). Assume that initially Q = 0. [4 marks]



(a)



(b)

b) Explain the following flip-flop timing parameters

i) Setup Time and Hold Time [3 marks]

ii) Clock transition times [2 marks]

c) Using a well labeled diagram and a truth table describe the operation of a subtractor circuit [6 marks]

d) Using D-Flip flops and waveforms explain the working of a 4-bit SISO shift register [5 marks]

QUESTION THREE [20 MARKS]

a) Illustrate the application of a flip flops in frequency division in digital circuits [6 marks]

b) List any three applications of decoders [3 marks]

c) Explain the following terms;

i) Combinational logic circuit [3 marks]

ii) Sequential logic circuits [3 marks]

d) Design a mode 12 counter [5 marks]

QUESTION FOUR [20 MARKS]

a) A logic signal is required to give an indication when:

- The supply to an oven is on, and

- The temperature of the oven exceeds 210°C, or
- The temperature of the oven is less than 190°C.

Devise a logic circuit using **NAND**-gates only to meet these requirements. [4 marks]

b) Describe any two applications of multiplexers [4 marks]

c) Explain the following terms in relation to logic families;

i) Noise immunity [2 marks]

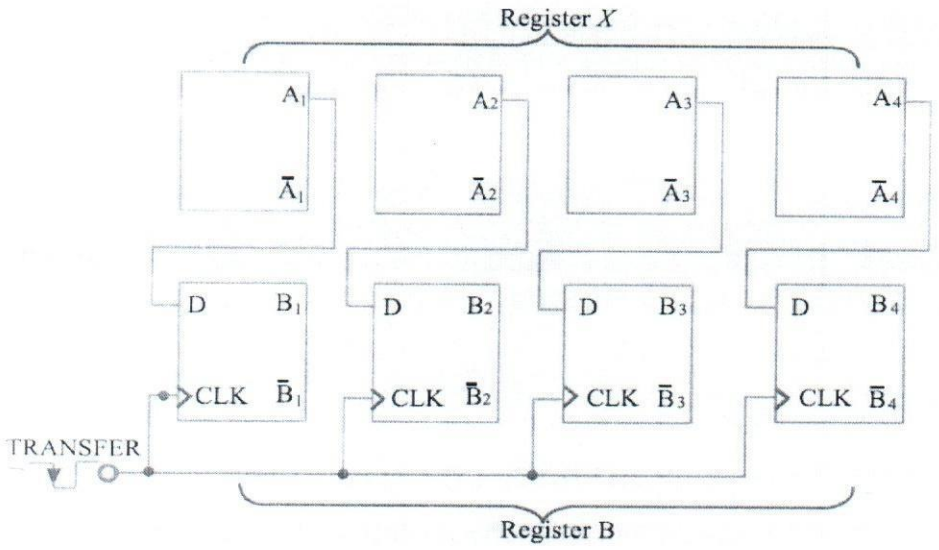
ii) Noise margin [2 marks]

d) Standardize the expression X = A'B + ABC + BD' [4 marks]

e) Implement a truth table that satisfies the result in 4(d) above [4 marks]

QUESTION FIVE [20 MARKS]

a) Describe how data transfer is achieved in the circuit below [5 marks]



b) A chemical processing plant system is required to turn on automatically whenever the chemical levels in any two or more of four cylinders A, B, C, and D falls below a preset level. Each cylinder is provided with a level detector that generated a high voltage whenever the water level in that cylinder is low

i) Use a truth table to determine the logic function performed [5 marks]

ii) Obtain Boolean equation for the required circuit and simplify using K-map [5 marks]

iii) Implement the results in (ii) above using appropriate logic gates [5 marks]