(*Knowledge for Development*)

KIBABII UNIVERSITY

UNIVERSITY EXAMINATIONS
2019/2020 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS
YEAR TWO SEMESTER ONE EXAMINATIONS

FOR THE DEGREE OF
BACHELOR OF SCIENCE COMPUTER SCIENCE

COURSE CODE: **CSC 211**

COURSE TITLE: **DIGITAL ELECTRONICS II**

DATE: 05/02/2021 **TIME: 02.00 P.M - 04.00P.M**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE [COMPULSORY] [30 MARKS]

a) (i) What is a full adder **(1mark)**

(ii) The logic diagram of Fig. 1 performs the function of a very common arithmetic building block. Identify the logic function. **(4 marks)**

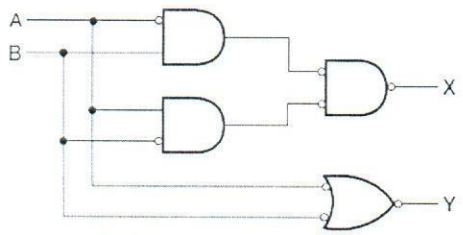


Fig.1

b) Draw a 4-1 multiplexer circuit diagram and derive its truth table **(5 marks)**

c) Outline any five applications of flip flops **(5 marks)**

d) (i) Mention any three types of D/A converters **(3 marks)**
(ii) An eight-bit D/A converter has a step size of 20 mV. Determine the full-scale output and percentage resolution. **(6 marks)**

e) (i) What is a microprocessor **(1mark)**

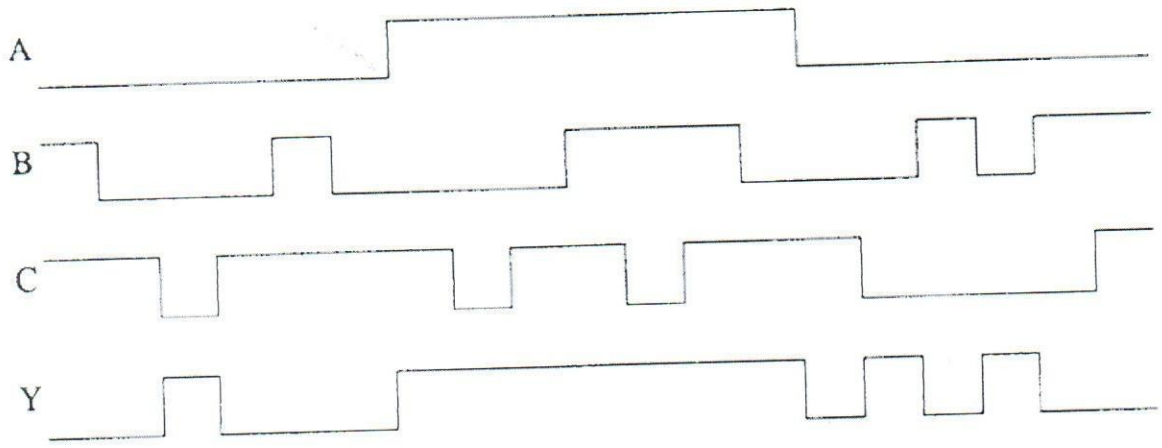
(ii) List of any five desirable characteristics of a microprocessor **(5 marks)**

QUESTION TWO [20 MARKS]

a) Distinguish between asynchronous and synchronous systems **(2 marks)**

b) Draw a well-labelled diagram of a clocked RS flip-flop using NAND gates. Derive its truth table **(3 marks)**

c) Given the timing diagram in Figure below, write out the truth table for the circuit responsible for it, the Boolean equation describing its operation and draw the actual circuit. **(12 marks)**



QUESTION THREE [20 MARKS]

a) Distinguish between a multiplexer and an encoder **(2 marks)**

b) A 3-bit binary number is represented as $A_2\ A_1\ A_0$, where A_0 is the LSB. Design a logic circuit which will produce a HIGH output whenever the binary number is either 1, 2, 4 or 7. Implement the circuit using a 1 to 4 MUX . **(3 marks)**

c) Show how gated-SR flip-flop can be modified to operate as a D flip-flop and draw the truth table for D flip-flop. **(7 marks)**

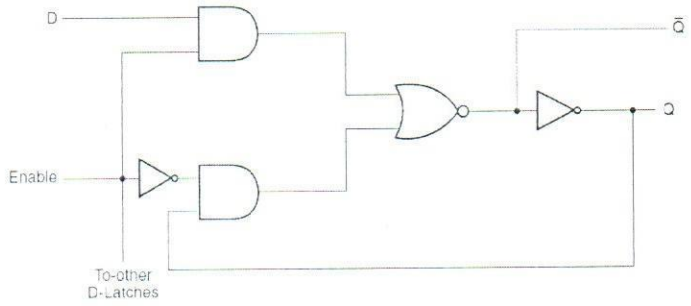
d) Write out the truth table for the 4-1ine-to-2-1ine encoder that takes a four-line decimal signal and converts it to binary code. Design and draw the circuit to implement this encoder. **(8 marks)**

QUESTION FOUR [20 MARKS]

a) Determine the size of the PROM required for implementing the following logic circuits:
(i) a binary multiplier that multiplies two four-bit numbers; **(2 marks)**
(ii) a dual 8-to-1 multiplexer with common selection inputs; **(2 marks)**
(iii) a single-digit BCD adder/subtractor with a control input for selection of operation. **(4 marks)**

b) Design a mod-10 binary up-counter using negative edge JK flip-flops with active- LOW clear. **(8 marks)**

c) Fig.2 below shows the internal logic circuit diagram of one of the four D latches of a four-bit D-latch in IC 7475.
(i) Give an argument to prove that the Q output will track the D input only when the ENABLE input is HIGH. **(2 marks)**
(ii) Prove that the Q output holds the value it had just before the ENABLE input went LOW during the time the ENABLE input is LOW. **(2 marks)**



QUESTION FIVE [20 MARKS]

a) Briefly explain the desirable characteristics of a digital to analogue converter (DAC) **(6 marks)**

b) Using a well-labelled schematic diagram, explain how a weighted binary resistance summing amplifier functions as a digital-to-analog converter (DAC). **(9 marks)**

c) State any five applications of D/A converters **(5 marks)**