(Knowledge for development)

KIBABII UNIVERSITY

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UNIVERSITY EXAMINATIONS
2019/2020 ACADEMIC YEAR

SPECIAL/SUPPLEMENTARY EXAMINATIONS
YEAR THREE SEMESTER TWO EXAMINATIONS

FOR THE DEGREE OF
BACHELOR OF SCIENCE
(COMPUTER SCIENCE)

COURSE CODE : CSC 353E

COURSE TITLE : DIGITAL SYSTEMS DESIGN

DATE: 11/02/2021 **TIME: 11.00 A.M – 01.00 P.M**

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTIONS ONE AND ANY OTHER TWO.

QUESTION ONE [COMPULSORY] [30 MARKS]

(a) (i) State the meaning of the term "digital system" and "analog system" with reference to data storage? **[4 marks]**

(ii) Differentiate between flip-flops and registers as used in the design of digital systems **[4 marks]**

(b) Field Programmable Gate Array (FPGA) is one type of semiconductor logic chip which can be programmed to become almost any kind of system or digital circuit.

(i) Using block diagram, briefly describe and explain the main building blocks of the architecture of FPGA **[9 marks]**

(ii) List three common applications of FPGA **[3 marks]**

(c) A digital module has clocked 8-bit data input bus and 16-bit counter output with a directional data bus. Write a code representation of the digital module **[3 marks]**

(d) Briefly explain the role of register transfer level - RTL in hardware description language **[3 marks]**

(e) Briefly state the meaning of logic simulation and synthesis as used in Hardware Description Language (HDL) for designing digital systems **[4 marks]**

QUESTION TWO [20 MARKS]

(a) (i) Define an Algorithmic State Machine (ASM)? **[1 marks]**

(ii) Define the following terms used in ASM method **[4 marks]**

a. State name
b. Decision box
c. Conditional output box
d. Data Path

(iii) ASM design method is composed of the five steps. List the steps. **[5 marks]**

(b) Explain the term state transition table and illustrate the state transition in a diagram form **[6 marks]**

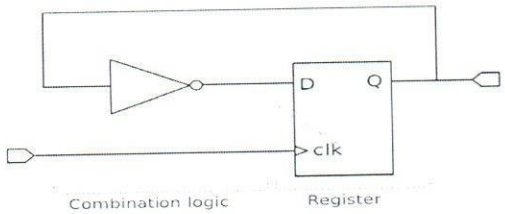
(c) (i) Discuss the role of "control logic" in a hierarchical state machines **[2 marks]**

(ii) Control unit design and implementation in sequential circuits can be done by two general methods. List and briefly describe the two methods. **[2 marks]**

QUESTION THREE [20 MARKS]

(a) Differentiate between "flip-flops" and "registers" as used in the design of digital systems **[4 marks]**

(b) The diagram below is a simple circuit with the output toggling at each rising edge of the input. The inverter forms the combinational logic in this circuit, and the register holds the state. Describe the circuit using a VHDL code **[4 marks]**



(c) State the role of port declaration and highlight three ways in which port declaration is implemented **[4 marks]**

(d) Briefly describe a "Loop Statement" as used in Hardware Description Language **[2 marks]**

(e) Loop statements comes with "For, While and Do loop" statements. Describe the use of each of the three statements and a syntax for each case. **[6 marks]**

QUESTION FOUR [20 MARKS]

(a) Explain the difference between programmable logic arrays (PLAs) and field programmable gate arrays (FPGAs) **[3 marks]**

(b) Programmable logic arrays (PLAs) implement two-level combinational logic in sum-of-products form. Using block diagram, briefly describe architecture of PLA **[6 marks]**

(c) Explain the role of gate level simulation applicable in FPGA **[2 marks]**

(d) Explain the difference between latches and flip-flops in asynchronous digital logic design **[2 marks]**

(e) Define the term "hazard" and explain the cause of hazards in asynchronous sequential circuits **[3 marks]**

(f) Discuss the differences between synchronous and asynchronous digital circuits **[4 marks]**

QUESTION FIVE [20 MARKS]

(a) Define the term "logic synthesis" applicable in design of digital systems? **[2 marks]**

(b) List two advantages of optimization of the design of digital systems by converting high-level design to gates through synthesis tools **[2 marks]**

(c) Verilog Hardware Description Language has two primary data types. State and briefly describe the two data types **[2 marks]**

(d) Every signal has a data type associated with it that is either explicitly declared or implicitly declared. Explain the meaning of explicit and implicit declaration **[2 marks]**

(e) Verilog HDL provided many different operators types. Briefly state and describe any four operators commonly used in Verilog. **[8 marks]**

(f) State the common register data type in Verilog whose functionality is as follows; **[4 marks]**

i. Interconnecting wire - no special resolution function
ii. Wired outputs OR together (models ECL)
iii. Unsigned variable
iv. Signed variable - 32 bits