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(Knowledge for Development)

KIBABII UNIVERSITY

UNIVERSITY EXAMINATIONS

2019/2020 ACADEMIC YEAR

END OF SEMESTER EXAMINATIONS

YEAR FOUR SEMESTER TWO

FOR THE DEGREE OF

COMPUTER SCIENCE

COURSE CODE: CSC 456E

COURSE TITLE: SEMICONDUCTOR DEVICES

DATE: 06/11/2020 **TIME: 2.00 P .M – 4.00 P.M**

INSTRUCTIONS:

ANSWER QUESTION ONE AND ANY OTHER TWO QUESTIONS

QUESTION ONE [COMPULSORY] [30 MARKS]

a) With a suitable example outline THREE types of particles in the atomic structure of semiconductor elements [6 marks]

b) Discuss THREE different classes of materials in relation to electrical properties. [6 marks]

c) Differentiate between passive and active component structures [2 marks]

d) Discuss THREE categories of contamination in cleanroom where modern semiconductor manufacturing is performed. For each contamination outline the control mechanism employed. [6 marks]

e) Outline TWO types of thyristors [2 marks]

f) Explain the following terms as used in semiconductor device processing technology:

i) Oxidation [2 marks]

ii) Diffusion [2 marks]

iii) Deposition [2 marks]

g) Differentiate between linear and switched mode power supplies [2 marks]

QUESTION TWO [20 MARKS]

a) Discuss any THREE key trends in semiconductor fabrication process [6 marks]

b) Describe Czochralski method of growing monocrystal ingots [5 marks]

c) Discuss THREE crystal defects in silicon [6 marks]

d) Differentiate Float zone technique from Czochralski method of growing monocrystal ingots. [3 marks]

QUESTION THREE [20 MARKS]

a) Outline FIVE stages of IC fabrication [10 marks]

b) Which device has most positive threshold voltage a depletion mode p-type MOSFET or an enhancement mode p-type MOSFET? Explain. [5 marks]

c) Outline FIVE major CMOS technology used to describe wafer fabrication process. [5 marks]

QUESTION FOUR [20 MARKS]

a) i) Outline the differences between diffusion and ion-implantation. Why ion-implantation has become largely used? [6 marks]

ii) Outline THREE side effects of ion implantation on the substrate material. [3 marks]

iii) Explain how the side effect in ii) is resolved. [3 marks]

b) i) Describe the term "epitaxy" as used in semiconductor device manufacturing. [2 marks]

ii) Outline TWO epitaxy growth methods [4 marks]

c) Outline TWO IC packaging techniques [2 marks]

QUESTION FIVE [20 MARKS]

a) Outline THREE requirements for a good integrated circuit packaging [6 marks]

b) Discuss Tape Automated Bonding as an interconnect attachment technique [6 marks]

c) Outline FOUR functions of IC packaging [8 marks]